AMENDMENTS TO THE DRAWINGS

Formal replacement drawings have been submitted herewith that include an amendment to Figure 2 for the inclusion of previously missing reference number 202.

AMENDMENTS TO THE CLAIMS

1. (currently amended) A processing system comprising:

a processor that is adapted to write compressed data;

a volatile memory device coupled to communicate with the processor;

a non-volatile memory device coupled to ~~communicate with~~ receive the compressed data from the processor ~~and the volatile memory device~~, ~~wherein~~ the non-volatile memory device further coupled to transfer ~~transfers~~ data to the volatile memory device; and

a decompression circuit provided in the non-volatile memory device to decompress the data being transferred ~~while transferring~~ to the volatile memory device.

2. (original) The processing system of claim 1 wherein the volatile memory device initiates the data transfer.

3. (original) The processing system of claim 1 wherein the non-volatile memory device is a flash memory device.

4. (original) The processing system of claim 1 wherein the processor is coupled to store compressed data in the volatile memory device.

5. (original) The processing system of claim 1 wherein volatile memory device is a dynamic random access memory.

6. (currently amended) A processing system comprising:

a processor that is adapted to write compressed data;

a synchronous memory device coupled to communicate with the processor via a synchronous bus;

a flash memory device coupled to ~~communicate with~~ receive the compressed data from the processor via a serial bus and communicate with the synchronous memory device, wherein the flash memory device transfers data to the synchronous memory device; and

a decompression circuit provided in the flash memory device to decompress the data while transferring to the synchronous memory device.

7. (original) The processing system of claim 6 wherein the synchronous memory device initiates the data transfer.

8. (original) The processing system of claim 7 wherein the synchronous memory device provides a system reset signal to the processor after the data is transferred from the flash memory device.

9. (original) The processing system of claim 6 wherein the synchronous memory device is an SDRAM.

10. (original) The processing system of claim 6 wherein the synchronous memory device is an RDRAM.

11 – 15 (cancelled)

16. (currently amended) A processor system power-up method comprising:

detecting a power-up condition with a reset controller and providing a reset signal to a synchronous memory;

using the synchronous memory, initiating a data transfer from a flash memory that comprises a decompression capability to the synchronous memory in response to the reset signal;

using the decompression capability of the flash memory, decompressing data stored in the ~~non-volatile~~ flash memory while transferring the data to the synchronous memory; and

providing a system reset signal from the synchronous memory to a processor after the data has been transferred.

17. (original) The method of claim 16 wherein the synchronous memory is coupled to the processor via a synchronous bus.

18. (currently amended) The method of claim ~~11~~ 16 wherein the wherein the synchronous memory device is either an SDRAM or an RDRAM.

19. (currently amended) A method of loading a synchronous dynamic random access memory (SDRAM) comprising:

using the SDRAM, initiating a data transfer from a flash memory to the synchronous dynamic random access memory; and

decompressing data stored in the ~~non-volatile~~ flash memory while transferring the data to the synchronous dynamic random access memory; and

providing a system reset signal from the SDRAM to a processor after the data has been transferred.

20. (currently amended) A method of loading a synchronous rambus dynamic random access memory (RDRAM) comprising:

using the RDRAM, initiating a data transfer from a flash memory, comprising a decompression capability, to the synchronous rambus dynamic random access memory in response to the reset signal;

using the decompression capability, decompressing data stored in the ~~non-volatile~~ flash memory while transferring the data to the synchronous rambus dynamic random access memory; and

providing a system reset signal from the RDRAM to a processor after the data has been transferred.